APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,889	08/06/2001	Rasekh Rifaat	A0312/7412 WRM/IB	6192

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EXAMINER
BURD, KEVIN MICHAEL

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 12/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>11 September 2003</u>.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-30* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a)☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: .

1.   This office action, in response to the amendment filed 9/11/2003, is a final office

action.

Response to Arguments

2.   The objection to the claims is withdrawn.

3.   Applicant's arguments filed 9/11/2003 have been fully considered but they are

not persuasive. Lomp discloses a single instruction of receiving inputs that comprise at

least a signal value (output of AMF 1710) and a dispreading code (PN1) as shown in

figure 17. The components of the instruction are received via two signal lines. The

signals are multiplied together to output a despread signal. Addition of this despread

signal and the output of despreader 1709 is done in unit 1718. The signal is stored while

being forwarded to the next downstream elements as shown in figure 17. These steps

take place in a digital signal processor shown in figure 17 comprising all the

components shown in figure 17. For these reasons and the reasons stated in the

previous office action, the rejections of the claims are maintain and stated below.

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public
> use or on sale in this country, more than one year prior to the date of application for patent in the United
> States.

2.   Claims 1-14 and 16-30 are rejected under 35 U.S.C. 102(b) as being anticipated

by Lomp et al (US 5,799,010).

Regarding claim 1, Lomp discloses a method of processing an input signal. In

figure 17, Lomp discloses an input signal and a PN sequence input to a despreader

1703 and a despread input signal is output. The input and PN signal are multiplied

together to output the despread signal. Lomp discloses a single instruction of receiving

inputs that comprise at least a signal value (output of AMF 1710) and a despreading

code (PN1) as shown in figure 17. The components of the instruction are received via

two signal lines. The signals are multiplied together to output a despread signal.

Addition of this despread signal and the output of despreader 1709 is done in unit 1718.

The signal is stored while being forwarded to the next downstream elements as shown

in figure 17. These steps take place in a digital signal processor shown in figure 17

comprising all the components shown in figure 17.

Regarding claim 2, Lomp further discloses, in figure 17, the output of the

despreader is added to the output of another despreader 1709 in the rotate/combine

unit 1718. The output from despreader 1709 is an output from a previous multiplication

(decoding).

Regarding claim 3, Lomp further discloses the despread code is shown in column

45, lines 55-65. This code can be divided by a factor of four to yield one-fourth the

amplitude as can any despread code.

Regarding claim 4, Lomp discloses, in column 45, lines 55-65, the despread

code comprises 2 bits comprising 1 real bit and 1 imaginary bit.

Regarding claim 5, Lomp further discloses the output signal of a shift register circuit is converted to an antipodal sequence where 0 maps into +1 and 1 maps into -1 (column 21, lines 63-66). The -1 represents a "set code bit" and the +1 represents a "clear code bit".

Regarding claim 6, Lomp further discloses, in column 45, lines 55-65, the input signal represents 16 bits.

Regarding claim 7, Lomp further discloses, in column 45, lines 55-65, the input signal represents 16 bits, 8 real bits and 8 imaginary bits.

Regarding claim 8, Lomp discloses a method of processing an input signal. In figure 17, Lomp discloses an input signal and a PN sequence input to a despreader 1703 and a despread input signal is output. The input and PN signal are multiplied together to output the despread signal. Lomp further discloses, in figure 17, the output of the despreader is added to the output of another despreader 1709 in the rotate/combine unit 1718. The output from despreader 1709 is an output from a previous multiplication. The output of the rotate/combine unit is processed further by downstream elements. Lomp discloses a single instruction of receiving inputs that comprise at least a signal value (output of AMF 1710) and a dispreading code (PN1) as shown in figure 17. The components of the instruction are received via two signal lines. The signals are multiplied together to output a despread signal. Addition of this despread signal and the output of despreader 1709 is done in unit 1718. The signal is stored while being forwarded to the next downstream elements as shown in figure 17.

These steps take place in a digital signal processor shown in figure 17 comprising all the components shown in figure 17.

Regarding claim 9, the multiplying takes place using two different PN codes as shown in figure 17.

Regarding claim 10, Lomp further discloses the despread code is shown in column 45, lines 55-65. This code can be divided by a factor of four to yield one-fourth the amplitude as can any despread code.

Regarding claim 11, Lomp discloses, in column 45, lines 55-65, the despread code comprises 2 bits comprising 1 real bit and 1 imaginary bit.

Regarding claim 12, Lomp further discloses the output signal of a shift register circuit is converted to an antipodal sequence where 0 maps into +1 and 1 maps into -1 (column 21, lines 63-66). The -1 represents a "set code bit" and the +1 represents a "clear code bit".

Regarding claim 13, Lomp further discloses, in column 45, lines 55-65, the input signal represents 16 bits.

Regarding claim 14, Lomp further discloses, in column 45, lines 55-65, the input signal represents 16 bits, 8 real bits and 8 imaginary bits.

Regarding claim 16, Lomp discloses an apparatus for processing an input signal. In figure 17, Lomp discloses an input signal and a PN sequence input to a despreader 1703 and a despread input signal is output. The input and PN signal are multiplied together to output the despread signal. This apparatus stores data in the elements and lines shown in figure 17. Lomp further discloses, in figure 17, the output of the

despreader is added to the output of another despreader 1709 in the rotate/combine

unit 1718. The output from despreader 1709 is an output from a previous multiplication.

Lomp discloses a single instruction of receiving inputs that comprise at least a signal

value (output of AMF 1710) and a dispreading code (PN1) as shown in figure 17. The

components of the instruction are received via two signal lines. The signals are

multiplied together to output a despread signal. Addition of this despread signal and the

output of despreader 1709 is done in unit 1718. The signal is stored while being

forwarded to the next downstream elements as shown in figure 17. These steps take

place in a digital signal processor shown in figure 17 comprising all the components

shown in figure 17.

Regarding claim 17, Lomp further discloses the despread code is shown in

column 45, lines 55-65. This code can be divided by a factor of four to yield one-fourth

the amplitude as can any despread code.

Regarding claim 18, Lomp discloses, in column 45, lines 55-65, the despread

code comprises 2 bits comprising 1 real bit and 1 imaginary bit.

Regarding claim 19, Lomp further discloses the output signal of a shift register

circuit is converted to an antipodal sequence where 0 maps into +1 and 1 maps into -1

(column 21, lines 63-66). The -1 represents a "set code bit" and the +1 represents a

"clear code bit".

Regarding claim 20, Lomp further discloses, in column 45, lines 55-65, the input

signal represents 16 bits.

Regarding claim 21, Lomp further discloses, in column 45, lines 55-65, the input

signal represents 16 bits, 8 real bits and 8 imaginary bits.

Regarding claim 22, Lomp discloses a method of processing an input signal. In

figure 17, Lomp discloses an input signal and a PN sequence input to a despreader

1703 and a despread input signal is output. The input and PN signal are multiplied

together to output the despread signal. Lomp further discloses, in figure 17, the output

of the despreader is added to the output of another despreader 1709 in the

rotate/combine unit 1718. The output from despreader 1709 is an output from a

previous multiplication. The output of the rotate/combine unit is processed further by

downstream elements. This method stores data in the elements and lines shown in

figure 17. As stated in column 45, lines 55-65, the input signal represents 16 bits, 8 real

bits and 8 imaginary bits. Lomp discloses a single instruction of receiving inputs that

comprise at least a signal value (output of AMF 1710) and a dispreading code (PN1) as

shown in figure 17. The components of the instruction are received via two signal lines.

The signals are multiplied together to output a despread signal. Addition of this

despread signal and the output of despreader 1709 is done in unit 1718. The signal is

stored while being forwarded to the next downstream elements as shown in figure 17.

These steps take place in a digital signal processor shown in figure 17 comprising all

the components shown in figure 17.

Regarding claim 23, Lomp further discloses the output signal of a shift register

circuit is converted to an antipodal sequence where 0 maps into +1 and 1 maps into -1

(column 21, lines 63-66). The -1 represents a "set code bit" and the +1 represents a "clear code bit".

Regarding claim 24, Lomp discloses, in column 45, lines 55-65, the despread code comprises 2 bits comprising 1 real bit and 1 imaginary bit.

Regarding claim 25, Lomp further discloses, in column 45, lines 55-65, the input signal represents 16 bits, 8 real bits and 8 imaginary bits.

Regarding claim 26, Lomp discloses this communication system is a spread spectrum multiple access communication system. This communication system is capable of use with wireless telephone systems.

Regarding claim 27, Lomp discloses a method of processing an input signal. In figure 17, Lomp discloses an input signal and a PN sequence input to a despreader 1703 and a despread input signal is output. The input and PN signal are multiplied together to output the despread signal. Lomp discloses, in column 45, lines 55-65, the despread code comprises 2 bits comprising 1 real bit and 1 imaginary bit. Lomp discloses a single instruction of receiving inputs that comprise at least a signal value (output of AMF 1710) and a dispreading code (PN1) as shown in figure 17. The components of the instruction are received via two signal lines. The signals are multiplied together to output a despread signal. Addition of this despread signal and the output of despreader 1709 is done in unit 1718. The signal is stored while being forwarded to the next downstream elements as shown in figure 17. These steps take place in a digital signal processor shown in figure 17 comprising all the components shown in figure 17.

Regarding claim 28, Lomp discloses a method of processing an input signal. In figure 17, Lomp discloses an input signal and a PN sequence input to a despreader 1703 and an despread input signal is output. The input and PN signal are multiplied together to output the despread signal. Lomp further discloses, in figure 17, the output of the despreader is added to the output of another despreader 1709 in the rotate/combine unit 1718. The output from despreader 1709 is an output from a previous multiplication. The output of the rotate/combine unit is processed further by downstream elements. This method stores data in the elements and lines shown in figure 17. As stated in column 45, lines 55-65, the input signal represents 16 bits, 8 real bits and 8 imaginary bits. Lomp discloses a single instruction of receiving inputs that comprise at least a signal value (output of AMF 1710) and a dispreading code (PN1) as shown in figure 17. The components of the instruction are received via two signal lines. The signals are multiplied together to output a despread signal. Addition of this despread signal and the output of despreader 1709 is done in unit 1718. The signal is stored while being forwarded to the next downstream elements as shown in figure 17. These steps take place in a digital signal processor shown in figure 17 comprising all the components shown in figure 17.

Regarding claim 29, the output from despreader 1709 is an output from a previous multiplication. The output of the rotate/combine unit is processed further by downstream elements.

Regarding claim 30, Lomp discloses, in column 45, lines 55-65, the despread code comprises 2 bits comprising 1 real bit and 1 imaginary bit.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications; please mark "EXPEDITED PROCEDURE" or for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).
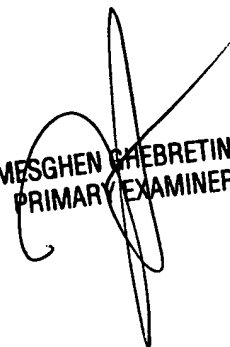
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Burd, whose telephone number is (703) 308-7034. The Examiner can normally be reached on Monday-Thursday from 9:00 AM - 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Kevin M. Burd
PATENT EXAMINER
12/5/03

TEMESGHEN GHEBRETINSAE
PRIMARY EXAMINER